LED Driver IC with Wide Input Voltage Range

Features

- Adjustable output current
- Universal 10VDC to 80 - 264VAC input
- Programmable clamped-mode switching
- Programmable switching OFF-time
- Internal 700V power MOSFET

Applications

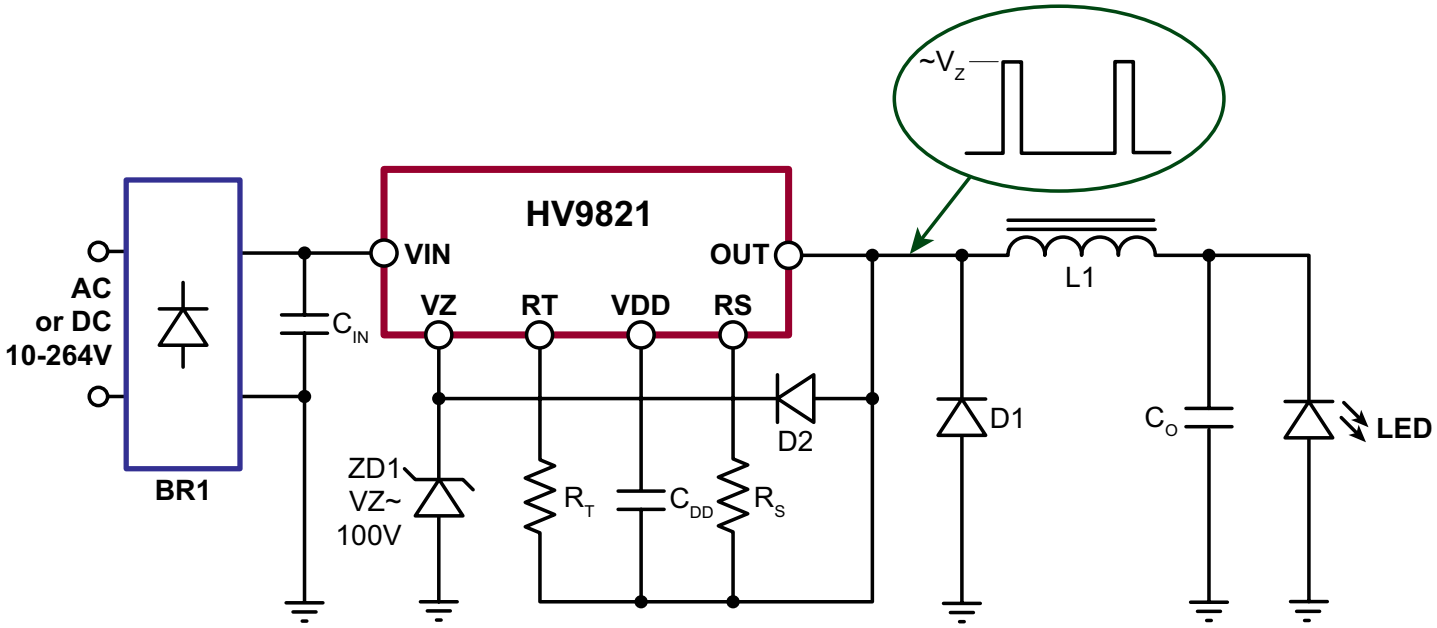
- LED backlighting
- Automation controls

General Description

The HV9821 is a clamped-mode high-side buck converter IC for driving a low-voltage LED load at constant current programmable up to 50mA (or higher, as permitted by power dissipation, etc.). The IC limits peak voltage at its switching output to a level programmed by connecting an external Zener diode. This feature ensures a reasonable on-time of the switch, while minimizing the conduction power loss of the HV9821. The IC operates with fixed off-time, programmable externally with a resistor.

The IC is equipped with over-temperature protection and packaged in a 19-Lead 7mm x 5mm DFN package.

Typical Application Circuit



Ordering Information

Part Number	Package Option	Packing
HV9821K7-G	19-Lead DFN (7x5)	364/Tray

-G denotes a lead (Pb)-free / RoHS compliant package

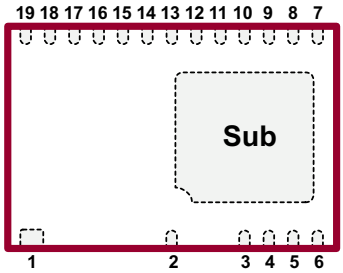
Absolute Maximum Ratings

Parameter	Value
Supply voltage, VDD	-0.3V to +13.5V
Gate driver, VZ	-0.7V to +13.5V
Other I/O	-0.3V to +13.5V
Supply current, IDD	5.0mA
RT current	2.0mA
Operating temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C
Power dissipation @ 25°C	3.3W

The power dissipation is given for the standard minimum pad without a heat slug, and based on θ_{ja} = 30°C/W

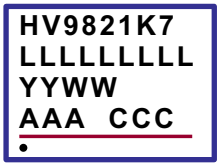
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pin Configuration



19-Lead DFN
(top view)

Product Marking



L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
____ = "Green" Packaging

Package may or may not include the following marks: Si or ⏻

19-Lead DFN

Typical Thermal Resistance

Package	θ_{ja}
19-Lead DFN	30°C/W

Electrical Characteristics

(Unless otherwise specified: All voltages referenced to OUT pin, T_A = 25ºC, R_T = 100kΩ, V_{IN} = 20V, RS = OUT, VZ open. Typical characteristics are specified at T_A = 25ºC.)

Sym	Description		Min	Typ	Max	Units	Conditions
Voltage Regulator (VIN, VDD)							
V_{DD}	Regulator output voltage	*	-	9.0	-	V	---
$V_{DD(UV)}$	VDD under-voltage threshold	-	-	3.0	-	V	V_{DD} falling ↓
$\Delta V_{DD(UV)}$	VDD hysteresis	-	-	0.4	-	V	V_{DD} rising ↑
I_{DDQ}	Operating supply current	-	-	-	500	µA	---
Output Switch (VIN, RS)							
BV	VIN breakdown voltage	*	700	-	-	V	---
R_{ON}	ON-resistance	*	-	60	100	Ω	---
I_{SAT}	VIN saturation current	* #	150	-	-	mA	V_{RS} = 1.0V
V_{GS}	VZ-to-RS voltage	-	-	2.0	-	V	I_{IN} = 50mA

Notes:

* *Specifications which apply over the full operating ambient temperature range of -40°C < T_A < +125°C, guaranteed by design and characterization.*

\# *Specifications guaranteed by design*

Electrical Characteristics

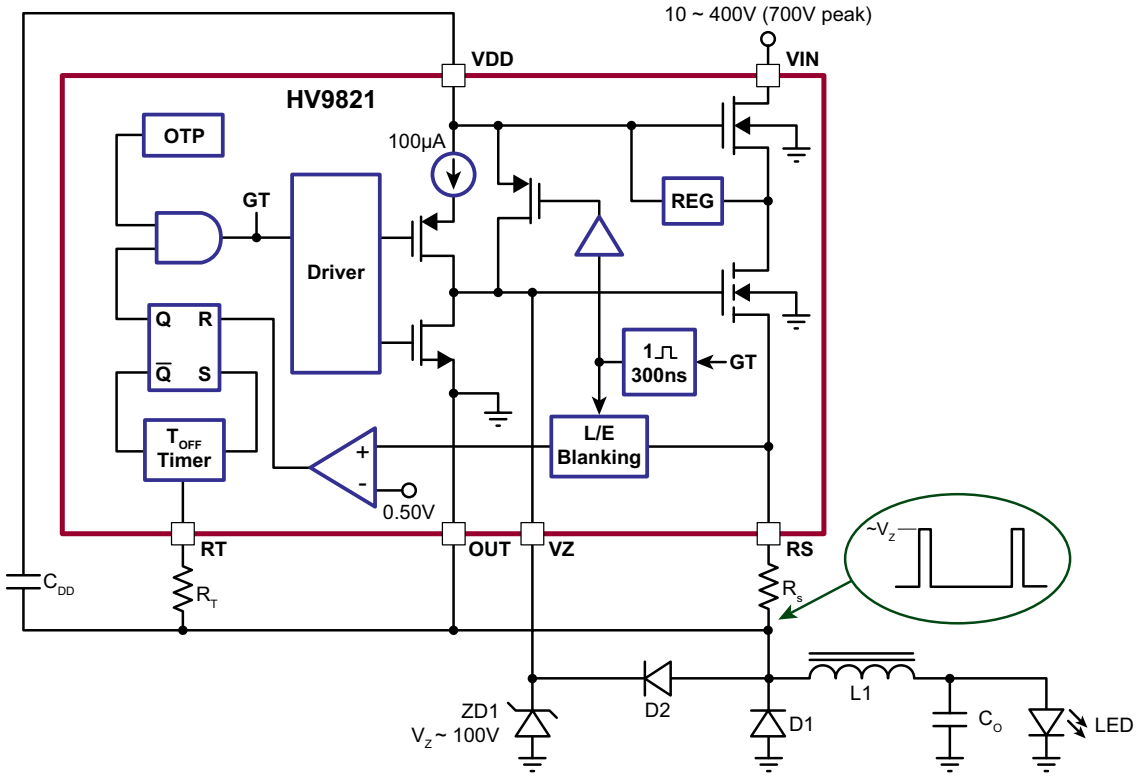
(Unless otherwise specified: All voltages referenced to OUT pin, T_A = 25ºC, R_T = 100kΩ, V_{IN} = 20V, RS = OUT, VZ open. Typical characteristics are specified at T_A = 25ºC.)

Sym	Description		Min	Typ	Max	Units	Conditions
Gate Driver (VZ)							
$I_{VZ(+)}$	VZ source current	*	-	-	10	mA	During T_{BLANK}, V_{DD} = 8.0V
$I_{VZ(-)}$	VZ sink current	*	-	6.5	-	mA	V_{DD} = 8.0V
$I_{VZ(BIAS)}$	VZ bias current	*	-	100	200	µA	V_{DD} = 8.0V
T_{OFF} Timer (RT)							
T_{OFF}	OFF time	-	8.8	10	11.2	µs	R_T = 100kΩ
$T_{OFF(MAX)}$	Maximum OFF time	-	80	100	120	µs	R_T = 1.0MΩ
Current Sense Comparator (RS)							
V_{TH}	Threshold voltage	*	0.40	0.50	0.60	V	---
T_{BLANK}	Leading edge blanking delay	*	200	-	400	ns	---
T_{DELAY}	Propagation delay RS to VIN	*	-	-	150	ns	---
Over-temperature Protection							
T_{OT}	Over temperature threshold	-	125	-	-	ºC	---
ΔT_{HYST}	Temperature hysteresis	-	-	20	-	ºC	---

Notes:

* *Specifications which apply over the full operating ambient temperature range of -40ºC < T_A < +125ºC, guaranteed by design and characterization.*

Functional Block Diagram



Power Topology

The HV9821 is a clamped-mode buck converter for driving a low-voltage LED load at a fixed current up to 50mA (or higher, as permitted by power dissipation, voltage drop and saturation current) from a wide range of input voltage of 10 to 700V. The IC generates a switching waveform of programmable amplitude V_{OUT} to accommodate the minimum duty cycle limitation. Since the input current can be determined as $I_{IN} = I_O \bullet D$, where $D = V_O / V_{OUT}$, the conduction losses due to the clamped mode are manageable:

$$P_{COND} = \left[V_O \bullet I_O + V_O \bullet I_{VZ(BIAS)} + I_{VZ(+)} \bullet (V_{OUT} - V_O) \bullet \frac{T_{BL}}{T_{OFF}} \right] \bullet \left(\frac{V_{IN}}{V_{OUT}} - 1 \right) + V_{IN} \bullet I_{DD(Q)}$$

where $V_{OUT} = V_Z - 2V$, $I_{DD(Q)} = 500\mu A(max)$, $I_{VZ(BIAS)} = 200\mu A(max)$, $I_{VZ(+)} = 10mA(max)$, and $T_{BL} = 400ns(max)$. The inductor value can be chosen in accordance with:

$$L_O = \frac{V_{OUT} \bullet T_{OFF}}{\Delta I_L}$$

where ΔI_L is the desired inductor current peak-to-peak ripple. The LED current is programmed by selecting the current sense resistor in accordance with the following equation:

$$R_{CS} = \frac{0.50V}{I_{OUT} - \frac{1}{2}\Delta I_L}$$

At low input voltage, parasitic resistances such as R_{ON} of the HV9821, DCR of the inductor, and sense resistor R_S start playing a major role. The 0.50V reference voltage can no longer develop at RS, and the HV9821 high-voltage switch remains in the on-state. At this condition, the internal regulator cannot power the IC, and the VDD voltage ramps down at the rate of $I_{DD(Q)}/C_{DD}$. When V_{DD} drops below 3.0V, the high-voltage switch turns off. The capacitor C_{DD} is charged to 3.4V. (See Figure 3.) Thus, at the described low input voltage condition, the HV9821 no longer maintains constant LED current, but rather enters a resistive mode of operation with periodical brief interruption to replenish charge in C_{DD}. The on-time between such interruptions is determined as $T_{ON} = 0.4V \bullet C_{DD}/I_{DD(Q)}$.

Voltage Clamp

The voltage limit at OUT is determined by breakdown voltage V_Z of an external Zener diode connected at VZ. The gate drive current of the internal power MOSFET is diverted into VZ, when the voltage reaches V_Z. Hence, the voltage at OUT becomes clamped to ~V_Z. For the duration of the leading-edge blanking delay of 300ns, this current can be up to 10mA. The current is further reduced to 100µA to minimize power dissipation in the Zener diode.

Connection of a Schottky diode between OUT and VZ prevents latch-up conditions due to parasitic charge redistribution in the switching circuit.

The VZ pin can be left open. In this case, the circuit shall function as a switching converter with the OUT voltage $V_{OUT} = V_{IN}$.

Regulator

The off state of the switch is used by an internal voltage regulator to derive the 9.0V supply at VDD from VIN for the control circuits.

Current Sense Comparator

The comparator terminates the gate driver on-state to pull the gate of the cascoded internal switching transistor to OUT, when the voltage at RS exceeds 0.50V. The 300ns leading-edge blanking delay prevents false tripping of the comparator.

OFF Timer

The IC operates with fixed off time of the power switch. This time duration is programmed with an external resistor at R_T in accordance with the equation $T_{OFF} = R_T \bullet 100pF$.

Over-Temperature Protection

The HV9821 is protected from over-temperature by turning the internal voltage regulator off at a temperature threshold greater than 125^{O}C. Minimum current shall be consumed by the IC until the junction temperature falls by 20^{O}C.

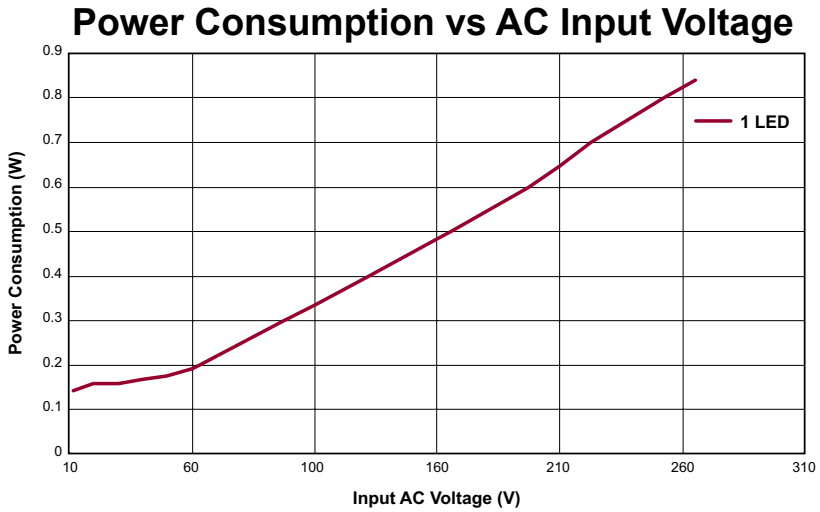


Figure 1. Power consumption as a function of the input AC voltage: V_{OUT} = 2.9V, V_Z = 91V

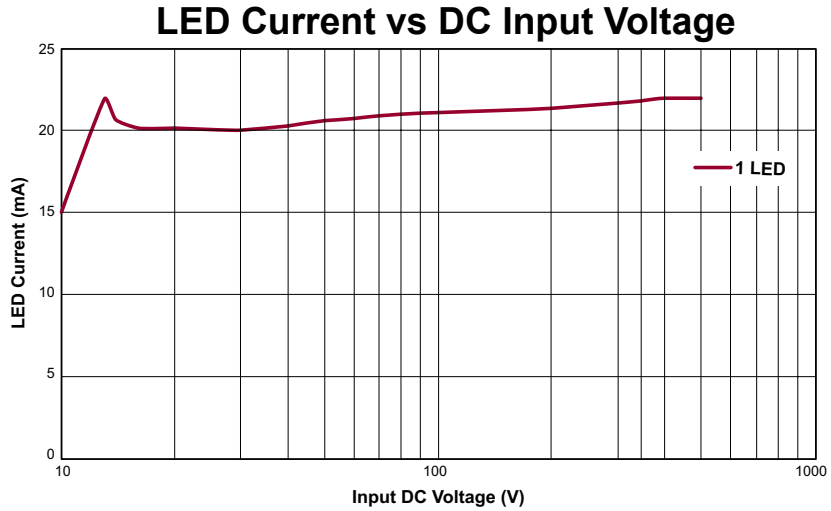


Figure 2. Input DC voltage regulation of LED current: V_{OUT} = 2.9V, V_Z = 91V

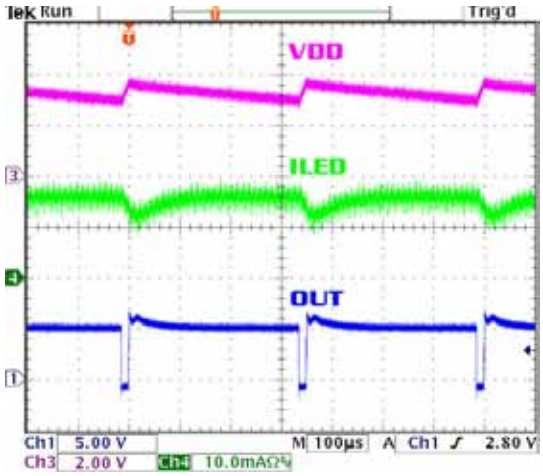


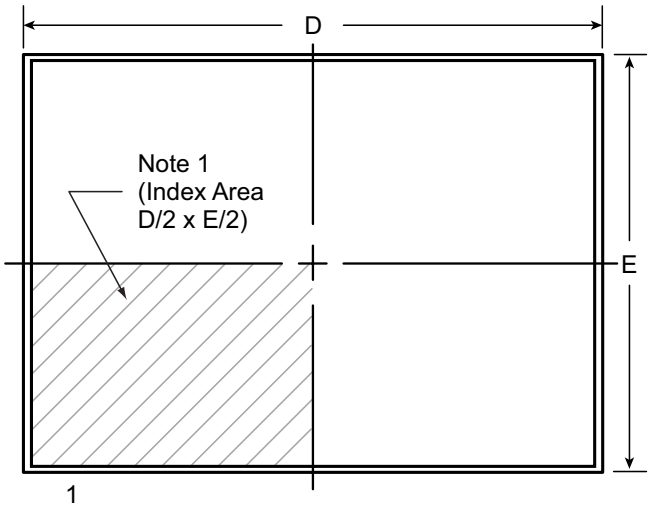
Figure 3. Low input voltage condition: V_{IN} = 10V, V_{OUT} = 2.9V.

Pin Description (19-Lead DFN)

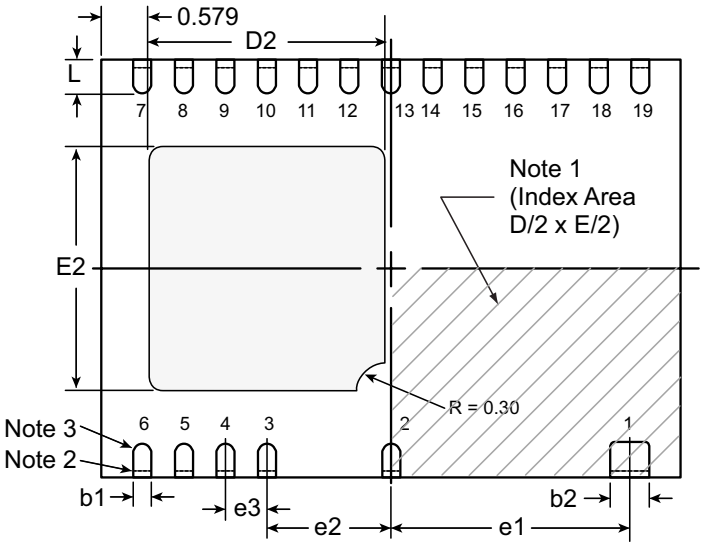
Pin	Name	Description
1	VIN	Input supply positive.
2	OUT	Circuit common.
3	RS	Source terminal of internal MOSFET, current sense resistor connection.
4	VZ	Gate driver output, Zener clamp connection.
5	RT	T_{OFF} programming pin, timing resistor connection.
6	VDD	Internally regulated 9V supply voltage to all circuits. A bypass capacitor to OUT of at least 1.0µF required.
7-19	OUT	Circuit common.
sub	OUT	Circuit common.

19-Lead DFN Package Outline (K7)

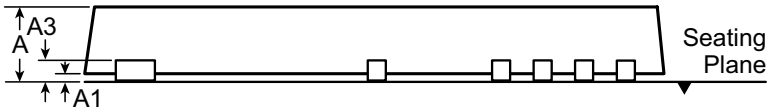
7.00x5.00mm body, 0.80mm height (max), 0.50mm pitch



Top View



Bottom View



Side View

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b1	b2	D	D2	E	E2	e1	e2	e3	L
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.20	0.42	7.00 BSC	2.692	5.00 BSC	2.802	2.875 BSC	1.50 BSC	0.50 BSC	0.30
	NOM	0.75	0.02		0.25	0.47		2.842		2.952				0.40
	MAX	0.80	0.05		0.30	0.52		2.942		3.052				0.50

Drawings not to scale.
Supertex Doc.#: *DSPD-19DFNK77X5P050, Version A053012.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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